



GENERAL DESCRIPTION



The ICS87322BI is a low skew, $\div 1/\div 2$ 3.3V LVPECL/ECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. Using multiplexed/redundant clock inputs the ICS87322BI is designed to translate most differential signal levels to LVPECL/ECL levels.

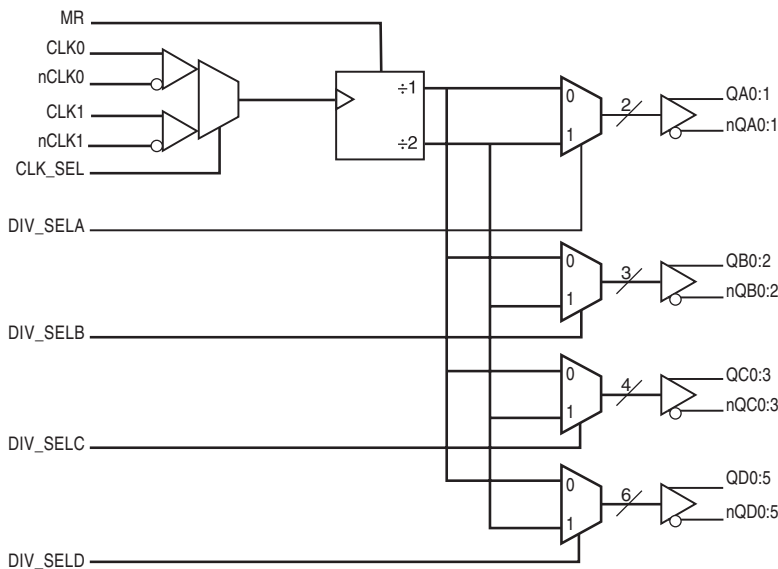
The CLK_SEL input selects between CLK0, nCLK0 and CLK1, nCLK1 as the active input. The divide select inputs, DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, control the output frequency of each bank. The outputs can be utilized in the $\div 1$, $\div 2$ or a combination of $\div 1$ and $\div 2$ modes. The master reset input can be used to reset the internal dividers and disable the clock outputs. Disabled outputs QA_x, QB_x, QC_x and QD_x will be forced low. Disabled outputs nQA_x, nQB_x, nQC_x and nQD_x will be forced high.

The ICS87322BI is characterized across the industrial temperature range and over the supply voltage range of 3V to 3.8V for LVPECL and -3.8V to -3V for LVECL/ECL. Guaranteed output and part to part skew characteristics make the ICS87322BI an excellent choice for clock generator and clock distribution applications demanding well defined performance and repeatability.

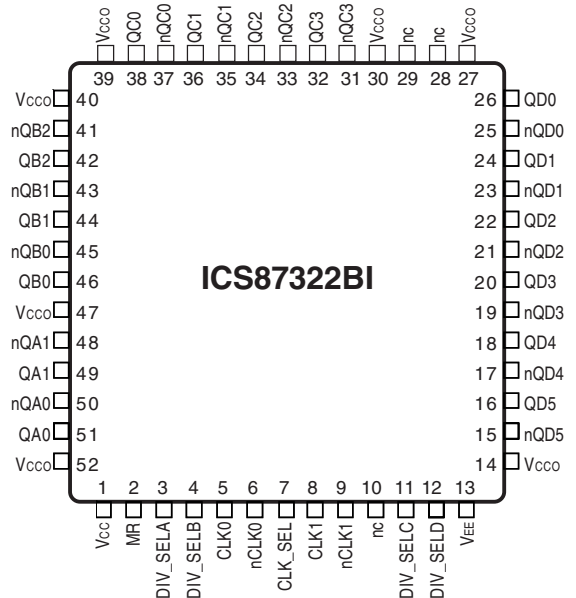
FEATURES

- 15 differential LVPECL outputs
- Selectable LVPECL differential clock inputs
- CLK0, nCLK0 and CLK1, nCLK1 can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: 750MHz (maximum)
- Output skew: 180ps (maximum)
- Bank skew: 65ps (maximum)
- Part-to-part skew: 500ps (maximum)
- LVPECL mode operating voltage supply range: $V_{CC} = 3V$ to 3.8V, $V_{EE} = 0V$
- ECL mode operating voltage supply range: $V_{CC} = 0V$, $V_{EE} = -3.8V$ to -3V
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



52-Lead LQFP

10mm x 10mm x 1.4mm package body

Y package

Top View



TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|-------------------------------|------------------|--------|----------|--|
| 1 | V _{CC} | Power | | Core supply pin. |
| 2 | MR | Input | Pulldown | Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels. |
| 3 | DIV_SELA | Input | Pulldown | Selects divide value for Bank A output as described in Table 3C. LVCMOS / LVTTTL interface levels. |
| 4 | DIV_SELB | Input | Pulldown | Selects divide value for Bank B output as described in Table 3C. LVCMOS / LVTTTL interface levels. |
| 5 | CLK0 | Input | Pulldown | Non-inverting differential LVPECL clock input. LVPECL interface levels. |
| 6 | nCLK0 | Input | Pullup | Inverting differential LVPECL clock input. LVPECL interface levels. |
| 7 | CLK_SEL | Input | Pulldown | Clock select. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTTL interface levels. |
| 8 | CLK1 | Input | Pulldown | Non-inverting differential LVPECL clock input. LVPECL interface levels. |
| 9 | nCLK1 | Input | Pullup | Inverting differential LVPECL clock input. LVPECL interface levels. |
| 10, 28, 29 | nc | Unused | | No connect. |
| 11 | DIV_SEL C | Input | Pulldown | Selects divide value for Bank C output as described in Table 3C. LVCMOS / LVTTTL interface levels. |
| 12 | DIV_SEL D | Input | Pulldown | Selects divide value for Bank D output as described in Table 3C. LVCMOS / LVTTTL interface levels. |
| 13 | V _{EE} | Power | | Negative supply pin. |
| 14, 27, 30, 39, 40, 47, 52 | V _{CCO} | Power | | Output supply pins. |
| 15, 16 | nQD5, QD5 | Output | | Differential output pair. LVPECL interface levels. |
| 17, 18 | nQD4, QD4 | Output | | Differential output pair. LVPECL interface levels. |
| 19, 20 | nQD3, QD3 | Output | | Differential output pair. LVPECL interface levels. |
| 21, 22 | nQD2, QD2 | Output | | Differential output pair. LVPECL interface levels. |
| 23, 24 | nQD1, QD1 | Output | | Differential output pair. LVPECL interface levels. |
| 25, 26 | nQD0, QD0 | Output | | Differential output pair. LVPECL interface levels. |
| 31, 32 | nQC3, QC3 | Output | | Differential output pair. LVPECL interface levels. |
| 33, 34 | nQC2, QC2 | Output | | Differential output pair. LVPECL interface levels. |
| 35, 36 | nQC1, QC1 | Output | | Differential output pair. LVPECL interface levels. |
| 37, 38 | nQC0, QC0 | Output | | Differential output pair. LVPECL interface levels. |
| 41, 42 | nQB2, QB2 | Output | | Differential output pair. LVPECL interface levels. |
| 43, 44 | nQB1, QB1 | Output | | Differential output pair. LVPECL interface levels. |
| 45, 46 | nQB0, QB0 | Output | | Differential output pair. LVPECL interface levels. |
| 48, 49 | nQA1, QA1 | Output | | Differential output pair. LVPECL interface levels. |
| 50, 51 | nQA0, QA0 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.



TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|--------------------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | CLKx, nCLKx | | 2 | | pF |
| | | CLK_SEL, DIV_SELx, MR | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

| Inputs | | Outputs | | | | | | | |
|--------|---------|---------|-----------|---------|-----------|---------|-----------|---------|-----------|
| MR | CLK_SEL | QA0:QA1 | nQA0:nQA1 | QB0:QB2 | nQB0:nQB2 | QC0:QC3 | nQC0:nQC3 | QD0:QD5 | nQD0:nQD5 |
| 1 | X | LOW | HIGH | LOW | HIGH | LOW | HIGH | LOW | HIGH |
| 0 | 0 | Active | Active | Active | Active | Active | Active | Active | Active |
| 0 | 1 | Active | Active | Active | Active | Active | Active | Active | Active |

TABLE 3B. INPUT CONTROL FUNCTION TABLE

| Inputs | |
|---------|-------------|
| CLK_SEL | Clock Input |
| 0 | CLK0, nCLK0 |
| 1 | CLK1, nCLK1 |

TABLE 3C. SELECT PIN FUNCTION TABLE

| Inputs | | | | Outputs | | | |
|--------|-------|-------|-------|---------|-----|-----|-----|
| SEL_A | SEL_B | SEL_C | SEL_D | QAx | QBx | QCx | QDx |
| 0 | 0 | 0 | 0 | ÷ 1 | ÷ 1 | ÷ 1 | ÷ 1 |
| 1 | 1 | 1 | 1 | ÷ 2 | ÷ 2 | ÷ 2 | ÷ 2 |

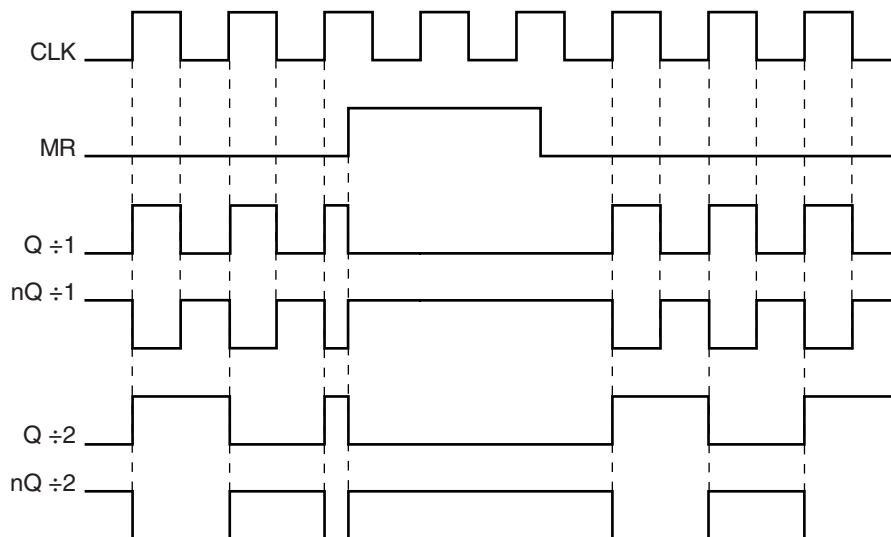


FIGURE 1. TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 42.3°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3V$ TO 3.8V, $T_A = -40^\circ C$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Core Supply Voltage | | 3.0 | 3.3 | 3.8 | V |
| V_{CCO} | Output Supply Voltage | | 3.0 | 3.3 | 3.8 | V |
| I_{EE} | Power Supply Current | | | | 160 | mA |
| I_{CCO} | Output Supply Current | | | | 98 | mA |

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3V$ TO 3.8V, $T_A = -40^\circ C$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|--|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | MR, CLK_SEL, F_SELA:F_SELD | 2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | MR, CLK_SEL, F_SELA:F_SELD | | | 0.8 | V |
| I_{IH} | Input High Current | MR, CLK_SEL, F_SELA:F_SELD $V_{CC} = V_{IN} = 3.8V$ | | | 150 | μA |
| I_{IL} | Input Low Current | MR, CLK_SEL, F_SELA:F_SELD $V_{IN} = 0V, V_{CC} = 3.8V$ | -5 | | | μA |

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3V$ TO 3.8V, $T_A = -40^\circ C$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|--------------------------------------|-----------------|------------------------------|---------|----------------|---------|
| I_{IH} | Input High Current | CLK0, CLK1 | $V_{CC} = V_{IN} = 3.8V$ | | 150 | μA |
| | | nCLK0, nCLK1 | $V_{CC} = V_{IN} = 3.8V$ | | 5 | μA |
| I_{IL} | Input Low Current | CLK0, CLK1 | $V_{IN} = 0V, V_{CC} = 3.8V$ | -5 | | μA |
| | | nCLK0, nCLK1 | $V_{IN} = 0V, V_{CC} = 3.8V$ | -150 | | μA |
| V_{PP} | Peak-to-Peak Voltage | | 0.15 | | 1.0 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | $V_{EE} + 1.5$ | | V_{CC} | V |
| V_{OH} | Output High Voltage, NOTE 3 | | $V_{CC} - 1.4$ | | $V_{CC} - 1.0$ | V |
| V_{OL} | Output Low Voltage, NOTE 3 | | $V_{CC} - 2.0$ | | $V_{CC} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Common mode voltage is defined as V_{IH} .

NOTE 2: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, CLK1 is $V_{CC} + 0.3V$.

NOTE 3: Outputs terminated with 50 Ω to $V_{CCO} - 2V$.

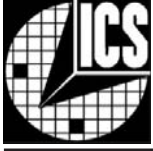


TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3V$ TO $3.8V$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|------------------------------|-----------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 750 | MHz |
| t_{PD} | Propagation Delay; NOTE 1 | | 1.5 | | 2.7 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 5 | | | | 180 | ps |
| | | $f = 212MHz$ | | | 150 | ps |
| $t_{sk(b)}$ | Bank Skew; NOTE 3, 5 | | | | 65 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 4, 5 | | | | 500 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 150 | | 600 | ps |

All parameters measured at $f \leq 750MHz$ unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{CCO}/2$.

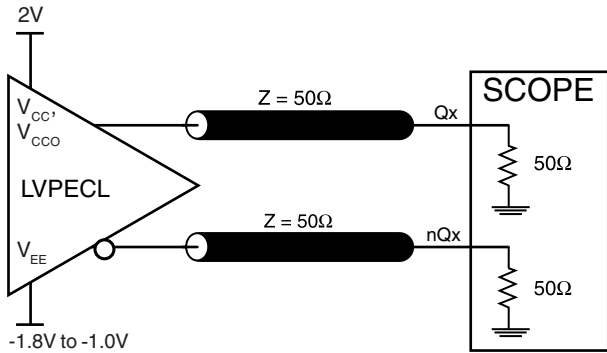
NOTE 3: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{CCO}/2$.

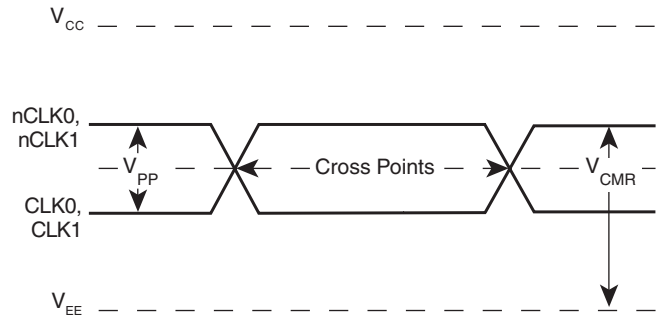
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.



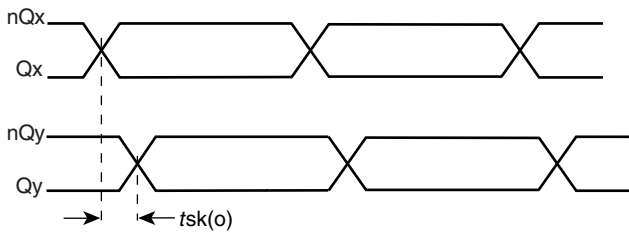
PARAMETER MEASUREMENT INFORMATION



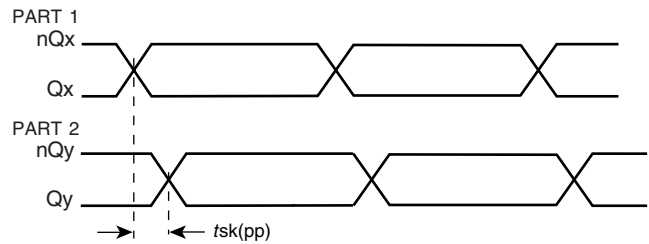
OUTPUT LOAD AC TEST CIRCUIT



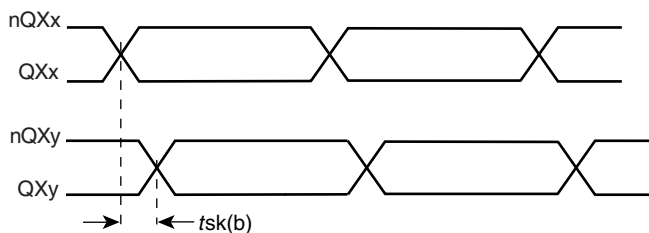
DIFFERENTIAL INPUT LEVEL



OUTPUT SKEW



PART-TO-PART SKEW

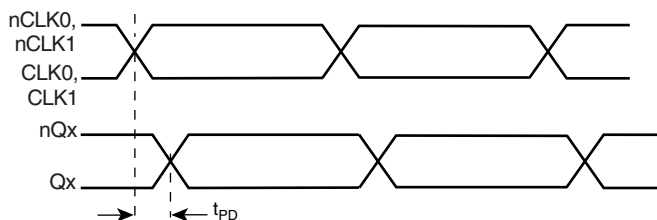


BANK SKEW

Where X = A, B, C or D



OUTPUT RISE/FALL TIME



PROPAGATION DELAY

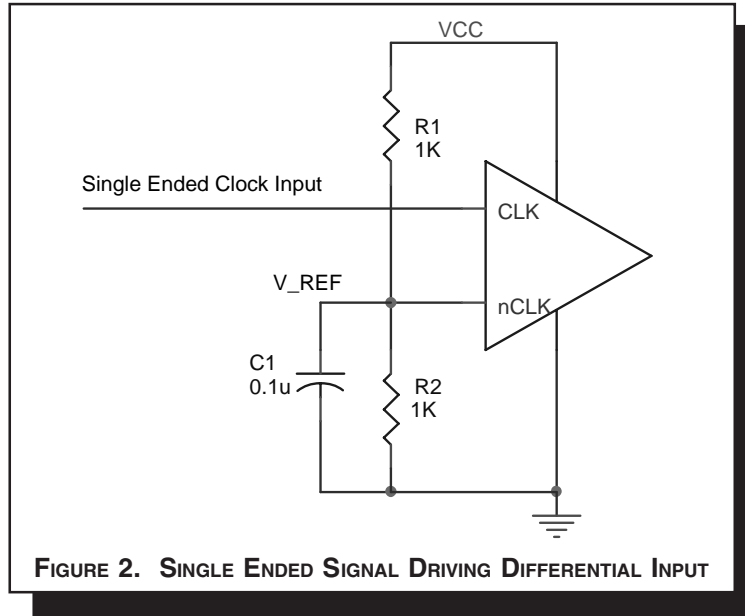


APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

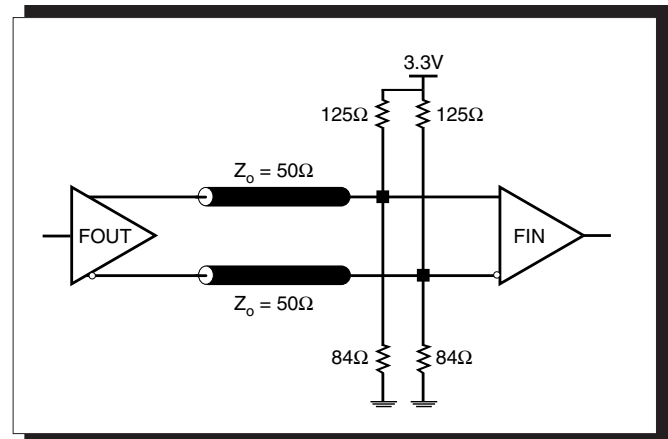
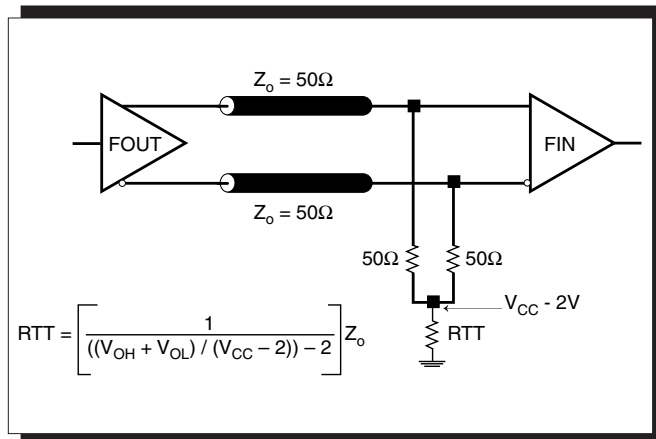


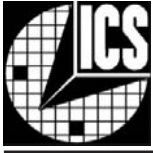
TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.





LVPECL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

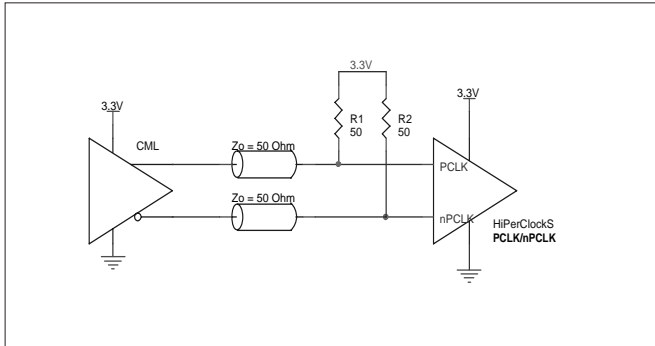


FIGURE 4A. HiPerClockS CLK/nCLK INPUT DRIVEN BY A CML DRIVER

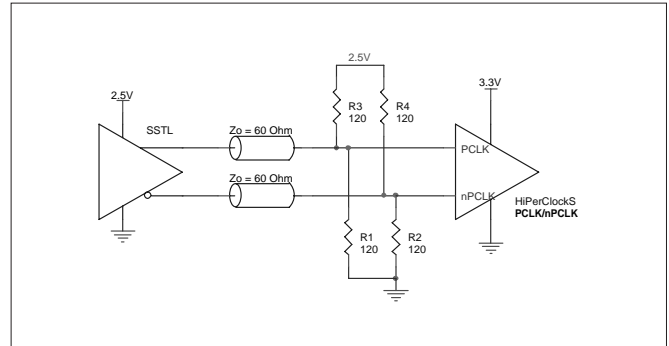


FIGURE 4B. HiPerClockS CLK/nCLK INPUT DRIVEN BY AN SSTL DRIVER

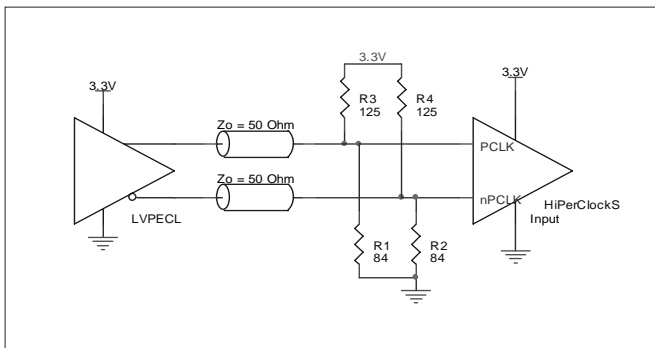


FIGURE 4C. HiPerClockS CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

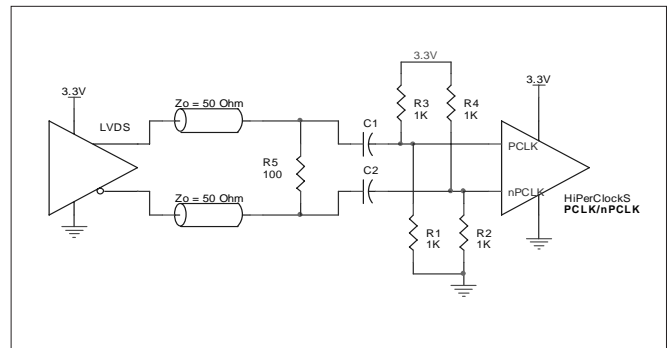


FIGURE 4D. HiPerClockS CLK/nCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

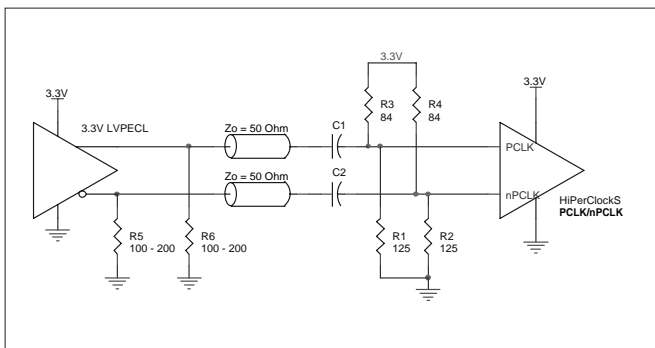


FIGURE 4E. HiPerClockS CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE



SCHEMATIC EXAMPLE

Figure 5 shows a schematic example of the ICS87322BI. In this example, the CLK0/nCLK0 input is selected. The input is driven by an LVPECL driver. All banks are set at $\div 2$. The decoupling capacitors should be physically located near the power pin. For ICS87322BI, the unused outputs can be left floating.

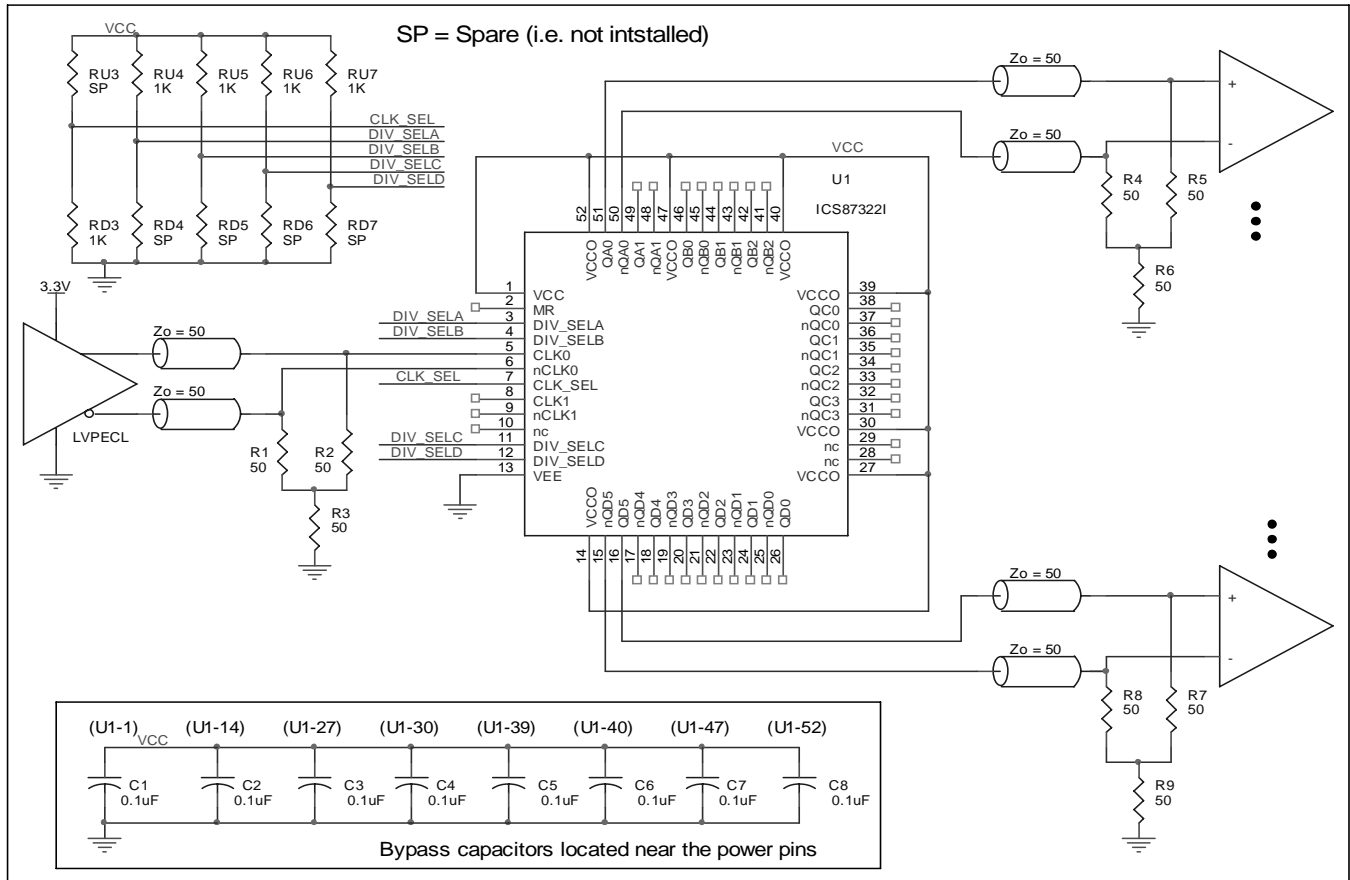


FIGURE 5. ICS87322BI SCHEMATIC EXAMPLE



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS87322BI. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS87322BI is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.8V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.8V * 160mA = 608mW$
- Power (outputs)_{MAX} = **30.2mW/Loaded Output pair**
If all outputs are loaded, the total power is $15 * 30.2mW = 453mW$

Total Power_{MAX} (3.8V, with all outputs switching) = $608mW + 453mW = 1061mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 36.4°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 1.061W * 36.4^\circ C/W = 123.6^\circ C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 52-PIN LQFP, FORCED CONVECTION

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 58.0°C/W | 47.1°C/W | 42.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 42.3°C/W | 36.4°C/W | 34.0°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.

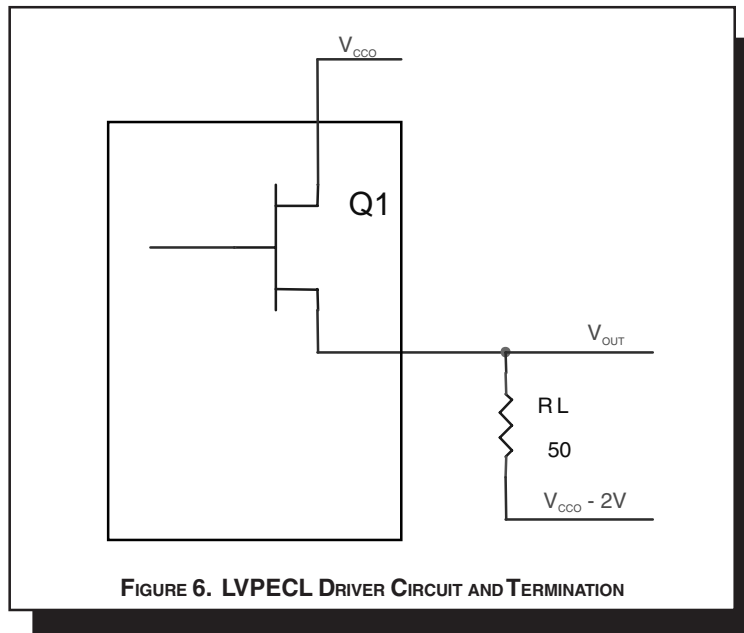


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 1.0V$

$$(V_{CCO_MAX} - V_{OH_MAX}) = 1.0V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$

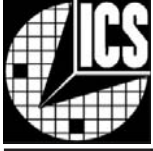
$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.
 Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 1V)/50\Omega] * 1V = 20.0mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = 30.2mW$



RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 52 LEAD LQFP

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 58.0°C/W | 47.1°C/W | 42.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 42.3°C/W | 36.4°C/W | 34.0°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87322BI is: 1331

Pin compatible with the MC100LVE222



PACKAGE OUTLINE - Y SUFFIX FOR 52 LEAD LQFP

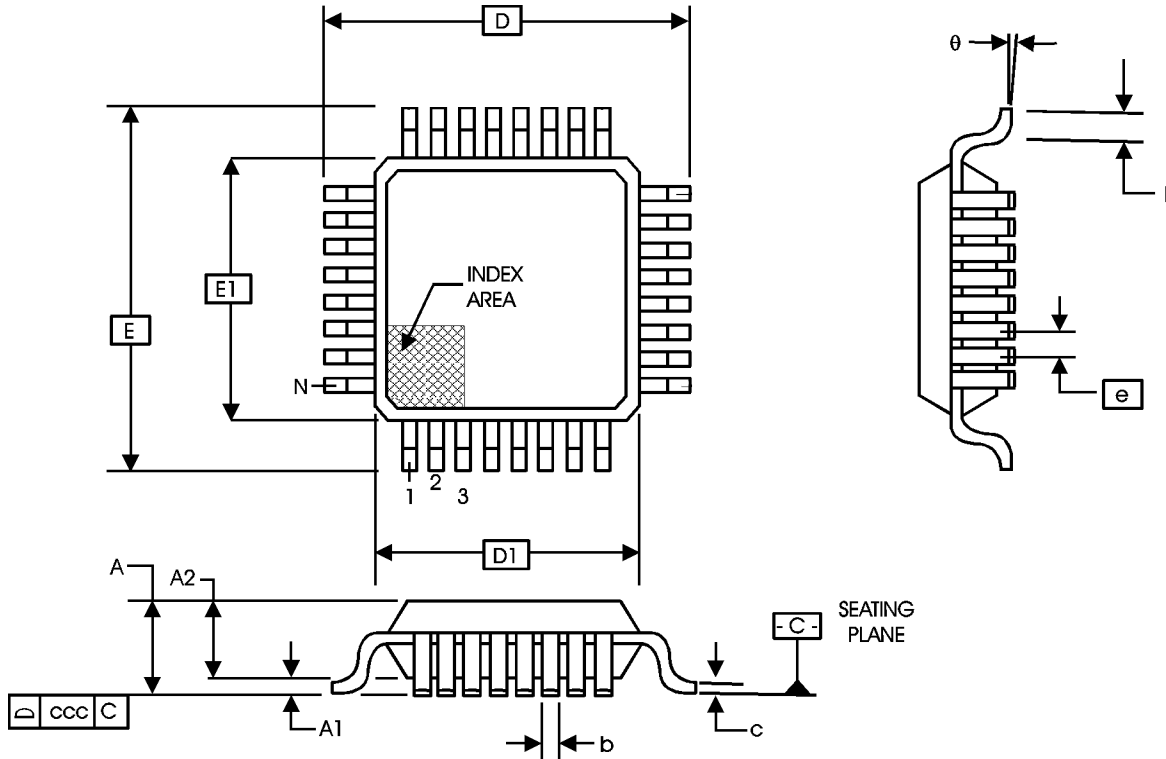


TABLE 8. PACKAGE DIMENSIONS

| JEDEC VARIATION | | | |
|-------------------------------|-------------|---------|---------|
| ALL DIMENSIONS IN MILLIMETERS | | | |
| SYMBOL | BCC | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 52 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.22 | 0.32 | 0.38 |
| c | 0.09 | -- | 0.20 |
| D | 12.00 BASIC | | |
| D1 | 10.00 BASIC | | |
| E | 12.00 BASIC | | |
| E1 | 10.00 BASIC | | |
| e | 0.65 BASIC | | |
| L | 0.45 | -- | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.08 |

Reference Document: JEDEC Publication 95, MS-026



Integrated
Circuit
Systems, Inc.

ICS87322BI

Low SKEW, $\div 1/\div 2$,
3.3V LVPECL/ECL CLOCK GENERATOR

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------------|--------------------------|--------------------|---------------|
| ICS87322BYI | ICS87322BYI | 52 Lead LQFP | tray | -40°C to 85°C |
| ICS87322BYIT | ICS87322BYI | 52 Lead LQFP | 500 tape & reel | -40°C to 85°C |
| ICS87322BYILF | ICS87322BYILF | 52 Lead "Lead-Free" LQFP | tray | -40°C to 85°C |
| ICS87322BYILFT | ICS87322BYILF | 52 Lead "Lead-Free" LQFP | 500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" to the part number are the Pb-Free configuration and are RoHS compliant.

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| REVISION HISTORY SHEET | | | | |
|------------------------|-------|------|--|---------|
| Rev | Table | Page | Description of Change | Date |
| B | T4A | 4 | Changed input levels to LVPECL throughout data sheet. | 4/6/04 |
| | T4B | 4 | Changed operating supply range from 2.375V to 3V throughout data sheet. Power Supply table - changed V_{CC} & V_{CCO} from 2.375V min. to 3V min. | |
| | T4C | 4 | LVC MOS table - deleted 2.625V test conditions. | |
| | | 4 | Changed Differential table to a LVPECL table. Deleted 2.625V test conditions. Revised V_{CMR} min. from $V_{EE} + 0.5V$ to $V_{EE} + 1.5V$ and max. from $V_{CC} - 0.85V$ to V_{CC} . | |
| | T5B | 5 | Deleted Table 5B, 2.5V AC Characteristics table. | |
| | | 6 | Revised Output Load AC Test Circuit Diagram, V_{EE} . | |
| | | 8 | Deleted Termination for 2.5V LVPECL Output. | |
| | | 9 | Changed Differential Clock Input Interface to LVPECL Clock Input Interface. (Now page 8.) | |
| B | T2 | 1 | Features section - added Lead-Free bullet. | 5/11/05 |
| | T9 | 2 | Pin Description Table - added pin 30 (V_{CCO}). | |
| | | 14 | Ordering Information Table - added Lead-Free part number. | |
| B | T9 | 14 | Ordering Information Table - added Lead-Free marking. | 6/9/05 |
| B | | 6 | Corrected Output Load AC Test Circuit Diagram - $V_{EE} = -1.8V$ to 1.0V from ...to -0.375V. | 6/20/05 |